B. S. T. J. BRIEFS

Extension of Multidimensional Polynomial Algebra to Domain Circuits with Multiple Propagation Velocities

By S. V. AHAMED

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I. INTRODUCTION

Multidimensional Polynomial Algebra[1] is a new technique for the analysis of circuits in which a finite and distinct time interval is necessary for the propagation of binary bits of data from one location to the next. These conditions exist specifically in magnetic domain circuits.[2,3] The algebra expands the basic concepts of the coding theorists,[4,5] and includes the representation of both time and space in the algebraic representation of data streams. A set of algebraic transformations[1] has been developed to correspond to the subfunctions in the circuit, and the overall function is thus modeled by a series of algebraic transformations. Such an analysis predicts the location and the value of all the binary positions at any prechosen instant of time, thus leading to the algebraic verification of the operation of a proposed circuit. In the foregoing technique for analysis, one velocity of propagation was assumed. However, the circuit designer may depend on more than one velocity for the successful operation of the circuit, and the technique suggested here accounts for different propagation velocities. Further, the analysis proposed determines the relationships between such velocities.

In discrete circuits, multiple velocities are generally derived from clock sources driven at different rates. The movement from one location to the adjoining location is finite, but the duration for the movement is derived from different clocks.

II. REPRESENTATION OF MULTIPLE CLOCKS

In Ref. 1 it was proposed that the number of clock cycles between a prechosen origin of time and a given instant of time be represented as the exponent of X; X being defined as the carrier of the time dimension. In multiple clock systems it is proposed that X be subscripted to denote the various clocks available in the system. Hence, if one adopts the

notation of Ref. 1 to denote the binary values of data bit positions (i.e., a_0 , a_1 , $\cdots$ a_{n-1} for the first, second, $\cdots$, nth, data bit positions), and to denote their spatial locations (i.e., $Y_k^{l_0}$, $Y_k^{l_1}$, $Y_k^{l_2}$, $\cdots$, $Y_k^{l_{n-1}}$ for the first, second, $\cdots$, nth locations in the kth element of a circuit), then a stream of data, n bits long after j_0 clock cycles at the first clock (denoted by the subscript 0 and X), may be represented as

$$u = X_0^{j_0} \sum_{i=0}^{i=n-1} a_i Y_k^{l_i}, \tag{1}$$

where l_i indicates the location number of the ith data position.

If this stream traverses for m_0 clock cycles in the forward direction, and is propagated at the first clock rate, then the final condition is

$$u = X_0^{j_0+m_0} \sum_{i=0}^{i=n-1} a_i Y_k^{l_i+m_0}. \tag{2}$$

Now if the data stream is propagated at a second clock rate (denoted by the subscript 1 for X) for m_1 clock cycles, the binary data is then represented as

$$u = X_0^{j_0+m_0} X_1^{m_1} \sum_{i=0}^{i=n-1} a_i Y_k^{l_i+m_0+m_1}. \tag{3a}$$

In general, the stream (1) after m_1 , m_2 , $\cdots$, m_j , $\cdots$ m_δ clock cycles at X_0 , X_1 , X_2 , $\cdots$, X_j $\cdots$, X_δ clocks, having been propagated from an element k to an element t, with their intersection located at Y_k^s and Y_t^0 , may be represented as

$$u = X_0^{j_0} \prod_{j=0}^{j=\delta} X_j^{m_j} \sum_{i=0}^{i=n-1} a_i Y_t^{\left(l_i + \sum_{j=0}^{j=\delta} m_j\right) - s}. \tag{3b}$$

Similar expressions for streams after looping, duplicating, logical gating, etc., may also be written (Ref. 1), and it is thus possible to model a series of functions in the circuit with multiple clocks by a series of algebraic equations, as was indicated for circuits with a single clock.

III. RELATION BETWEEN CLOCK RATES

The functional constraints on the circuit demand that bubble positions or streams be physically present at certain predefined locations and at preselected intervals of time. For example, it may be necessary

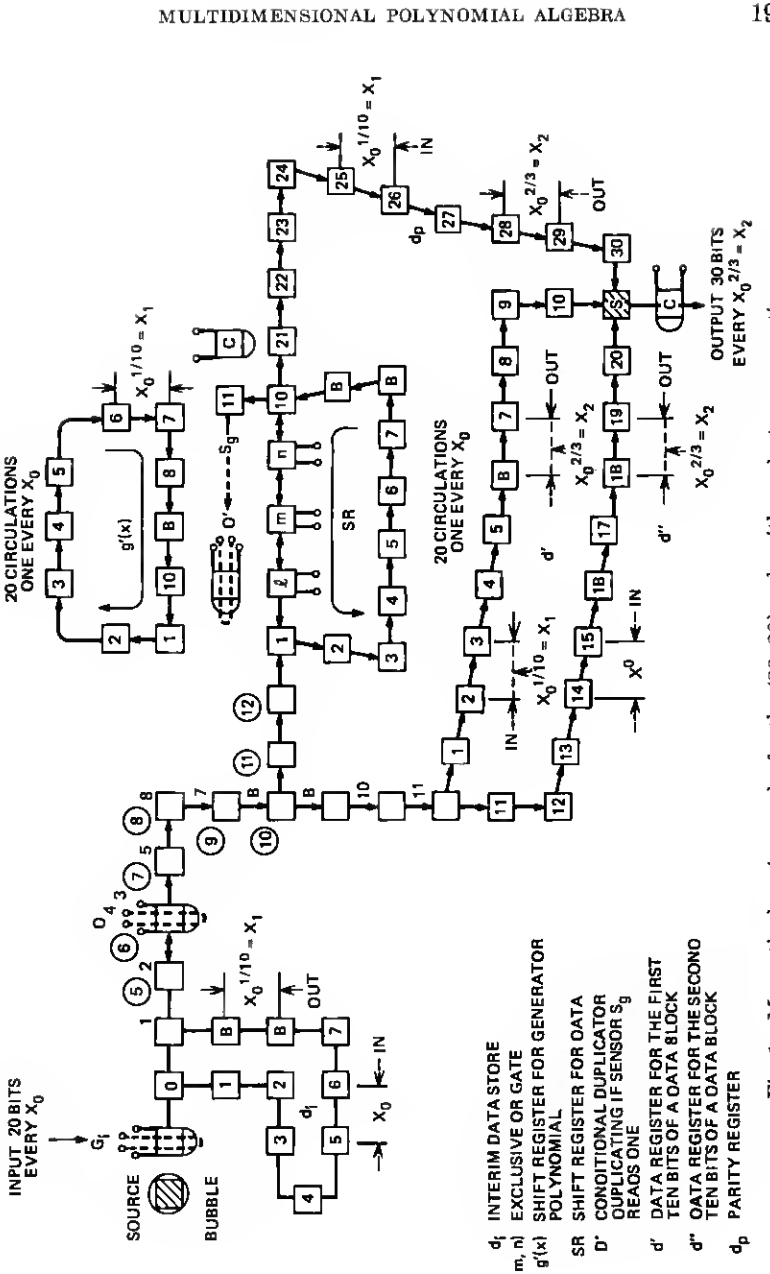

Fig. 1—Magnetic domain encoder for the (30, 20) code with conductor propagation.

for a binary stream to have completely circulated a loop (p periods) once and advanced one additional period* before the arrival of the next data bit.† If the incoming data is assumed to arrive every X_0 clock cycle, and the data in the p-period loop is being propagated one location every X_1 clock cycle, then one cycle at the rate X_0 should correspond to $(p + 1)$ cycles at the rate X_1. This leads to the conclusion that

$$X_1^{p+1} = X_0 , \tag{4}$$

and this equation should be construed to imply that the propagating clock at X_1 runs $(p + 1)$ times faster than the clock at X_0.

IV. Application of Algebra to the Design of a (30, 20) Domain Encoder

The application of the algebra to the design of a (30, 20) domain encoder[6] shown in Fig. 1 has yielded all the design parameters, the relation between different clocks, and the instants of synchronization of the various clocks to obtain a satisfactory operation of the encoder. It is foreseen that such an algebraic analysis of discrete circuits will help engineers to check the operation of the devices before they are constructed and reduce the debugging time once they have been made.

References

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* A period is defined as that unit of physical distance by which a binary position is propagated in one clock cycle at any rate X_0, or X_1, or X_2, etc.

† Such a requirement is placed in the magnetic domain encoders and decoders presented in Ref. 6.